LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An array substrate for use in a liquid crystal display device, comprising:

a gate electrode, a gate line and a gate pad electrode on a substrate, wherein all of the gate electrode, the gate line and the gate pad electrode have a double-layered structure including a first barrier metal layer and a first copper layer, wherein the first barrier metal layer is interposed between the substrate and the first copper layer, wherein sides of the first copper layer are inside of sides of the first barrier metal layer and wherein the first barrier metal layer and the first copper layer have a smooth taper shape without any steps on their sides;

a buffer layer between the substrate and the first barrier metal layer;

a gate insulation layer on the substrate covering the double-layered gate electrode, gate line and gate pad;

an active layer and an ohmic contact layer sequentially formed on the gate insulation layer and over the gate electrode;

a data line on the gate insulation layer crossing the gate line, source and drain electrodes contacting the ohmic contact layer, and a data pad electrode on the gate insulation layer, wherein all of the data line, the source and drain electrodes, and the data pad electrode have a double-layered structure including a second barrier metal layer and a second copper layer and wherein the second barrier metal layer is interposed between the substrate and the second copper layer, wherein each of the first and second barrier metal layers includes a metallic material that has a good adhesive characteristic to the substrate and prevents a reaction between the second copper layer and both the active layer and the ohmic contact layer, and wherein the metallic material is one of tantalum (Ta) and titanium (Ti);

a passivation layer formed on the gate insulation layer to cover the double-layered data line, source and drain electrodes, and data pad electrode, wherein the passivation layer has a drain contact hole exposing the drain electrode, a gate pad contact hole exposing the gate pad electrode, and a data pad contact hole exposing the data pad; and

a pixel electrode, a gate pad terminal and a data pad terminal all of which are formed of a transparent conductive material on the passivation layer.

2. (Original) The array substrate according to claim 1, wherein the gate electrode extends from the gate line and the gate pad electrode is at an end of the gate line.

3. (Original) The array substrate according to claim 1, wherein the source electrode extends from the data line, wherein the drain electrode is spaced apart from the source electrode, and wherein the data pad electrode is at an end of the data line.

4. (Original) The array substrate according to claim 1, wherein the pixel electrode is disposed in a pixel region defined by the crossing of the gate and data lines, wherein said pixel electrode contacts the drain electrode through the drain contact hole, wherein the gate pad terminal contacts the gate pad through the gate pad contact hole, and wherein the data pad terminal contacts the data pad through the data pad contact hole.

5-8 (Canceled)

9. (Original) The array substrate according to claim 1, further comprising a storage capacitor comprising:

a portion of the gate line;

the gate insulating layer as a dielectric layer; and

a double-layered capacitor electrode on the gate insulating layer and over the portion of the gate line;

wherein the double-layered capacitor electrode has the second barrier metal layer and the second copper layer.

10. (Original) The array substrate according to claim 9, wherein the double-layered capacitor electrode is connected in parallel with the pixel electrode through a contact hole formed in the passivation layer.

11. (Original) The array substrate according to claim 1, wherein the gate insulation layer is an inorganic material selected from a group consisting of silicon nitride and silicon oxide.

12. (Original) The array substrate according to claim 1, wherein the passivation layer is one of silicon nitride, silicon oxide, benzocyclobutene (BCB), acrylic resin, and double layers thereof.

13. (Canceled)

14. (Currently Amended) The array substrate according to claim [[~~13~~]]1, wherein the buffer layer is one of silicon nitride, silicon oxide, benzocyclobutene (BCB), acrylic resin, and double layers thereof.

15. (Currently Amended) The array substrate according to claim[[~~13~~]]1, wherein the metallic material has a good adhesive characteristic to the buffer layer.

16. (Canceled)

17. (Currently Amended) A method of forming an array substrate for use in a liquid crystal display device, comprising:

forming a gate electrode, a gate line and a gate pad electrode on a substrate, wherein all of the gate electrode, the gate line and the gate pad electrode have a double-layered structure including a first barrier metal layer and a first copper layer, wherein the first barrier metal layer is interposed between the substrate and the first copper layer, wherein sides of the first copper layer are inside of sides of the first barrier metal layer, and wherein the first barrier metal layer and the first copper layer have a smooth taper shape without any steps on their sides;

forming a buffer layer between the substrate and the first barrier metal layer;

forming a gate insulation layer on the substrate to cover the double-layered gate electrode, gate line and gate pad;

forming an active layer and an ohmic contact layer sequentially on the gate insulation layer and over the gate electrode;

forming a data line, source and drain electrodes and a data pad electrode, wherein the data line is on the gate insulation layer and crossed the gate line, wherein the source and drain electrodes contact the ohmic contact layer, wherein the data pad electrode is disposed on the gate insulation layer, and wherein all of the data line, the source and drain electrodes, the capacitor electrode and the data pad electrode have a double-layered structure including a second barrier

metal layer and a second copper layer and wherein the second barrier metal layer is interposed between the substrate and the second copper layer, wherein each of the first and second barrier metal layers includes a metallic material that has a good adhesive characteristic to the substrate and prevents a reaction between the second copper layer and both the active layer and the ohmic contact layer, and wherein the metallic material is any of tantalum (Ta) and titanium (Ti);

forming a passivation layer formed on the gate insulation layer to cover the double-layered data line, source and drain electrodes, and data pad electrode, wherein the passivation layer has a drain contact hole exposing the drain electrode, a gate pad contact hole exposing the gate pad electrode, and a data pad contact hole exposing the data pad; and

forming a pixel electrode, a gate pad terminal and a data pad terminal on the passivation layer using a transparent conductive material.

18. (Original) The method according to claim 17, wherein the gate electrode extends from the gate line and the gate pad electrode is at the end of the gate line.

19. (Original) The method according to claim 17, wherein the source electrode extends from the data line, wherein the drain electrode is spaced apart from the source electrode, and wherein the data pad electrode is at the end of the data line.

20. (Original) The method according to claim 17, wherein the pixel electrode is disposed in a pixel region defined by the crossing of the gate and data lines and contacts the drain electrode through the drain contact hole, wherein the gate pad terminal contacts the gate pad through the gate pad contact hole, and wherein the data pad terminal contacts the data pad through the data pad contact hole.

21-24 (Canceled)

25. (Currently Amended) The method according to claim ~~1~~ 17, wherein forming a data line, source and drain electrodes and a data pad electrode includes forming a double-layered capacitor electrode on the gate insulating layer and over the portion of the gate line, wherein the double-layered capacitor electrode has the second barrier metal layer and the second copper layer.

26. (Original) The method according to claim 25, wherein the double-layered capacitor electrode is connected in parallel with the pixel electrode through a contact hole that formed in the passivation layer.

27. (Original) The method according to claim 17, wherein the gate insulation layer is an inorganic material selected from a group consisting of silicon nitride and silicon oxide.

28. (Original) The method according to claim 17, wherein the passivation layer is one of silicon nitride, silicon oxide, benzocyclobutene (BCB), acrylic resin, or double layers thereof.

29. (Canceled)

30. (Currently Amended) The method according to claim ~~29~~ 17, wherein the buffer layer is one of silicon nitride, silicon oxide, benzocyclobutene (BCB), acrylic resin, or double layers thereof.

31. (Currently Amended) The method according to claim ~~29~~ 17, wherein the metallic material has a good adhesive characteristic to the buffer layer.

32. (Canceled)